

Please cancel claims 4, 5 and 9 and please replace claims 1, 6-7 and 11-12 with the following amended claims:

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- 1                    1.     (Twice Amended) A light-emitting thyristor matrix array  
B<sup>2</sup> 2     formed on a chip, comprising:
- 3                    N (N is an integer  $\geq 2$ ) three-terminal light-emitting thyristors  
4     arrayed in one line in parallel with the long side of the chip;
- 5                    a common terminal to which cathodes or anodes of the N light-  
6     emitting thyristors are connected;
- 7                    M (M is an integer  $\geq 2$ ) gate selecting lines; and
- 8                     $\{(N/M) + M\}$  bonding pads arrayed in one line in parallel with  
9     the long side of the chip,
- 10                   wherein the gate of kth light-emitting thyristor is connected to  
11     ith  $[i = \{(k-1) \text{ MOD } M\} + 1]$  gate-selecting line  $G_i$ , where "MOD" in an  
12     equation means modulo division,
- 13                   the anode or cathode which is not connected to the common  
14     terminal of the kth light-emitting thyristor is connected to jth  $[j = \{(k-i)/M\}$   
15     + 1] anode terminal  $A_j$  or cathode terminal  $K_j$ ,
- 16                   the number M of the gate-selecting lines is selected so as to  
17     satisfy the expression of  $L/\{(N/M) + M\} > p$  (L is a length of the long side of

B<sup>2</sup>  
cmf. 18 the chip and  $p$  is a critical value of the array pitch of the bonding pads) in  
19 order to decrease the area of the chip, and  
20 when a prime factor for  $N$  is 2 only, the number  $M$  of the gate-  
21 selecting lines is positive and is the smallest integer, next smaller integer, or  
22 third smaller integer that satisfies the expression  $L/\{(N/M)+M\} > p$ .

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B<sup>3</sup> 1 6. (Twice Amended) A light-emitting thyristor matrix array  
2 formed on a chip, comprising:

3  $N$  ( $N$  is an integer  $\geq 2$ ) three-terminal light-emitting thyristors  
4 arrayed in one line in parallel with the long side of the chip;

5 a common terminal to which cathodes or anodes of the  $N$  light-  
6 emitting thyristors are connected;

7  $M$  ( $M$  is an integer  $\geq 2$ ) gate-selecting lines; and

8  $\{(N/M)+M\}$  bonding pads arrayed in one line in parallel with the  
9 long side of the chip,

10 wherein the gate of  $k$ th light-emitting thyristor is connected to  
11  $i$ th [ $i = \{(k-1) \text{ MOD } M\} + 1$ ] gate-selecting line  $G_i$ , where "MOD" in an equation  
12 means modulo division,

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cont.

13 the anode or cathode which is not connected to the common  
14 terminal of the kth light-emitting thyristor is connected to jth [ $j = \{(k -$   
15  $i)/M\} + 1]$  anode terminal  $A_j$  or cathode terminal  $K_j$ ,

16 the number  $M$  of the gate-selecting lines is selected so as to  
17 satisfy the expression of  $L/\{(N/M) + M\} > p$  ( $L$  is a length of the long side of  
18 the chip and  $p$  is a critical value of the array pitch of the bonding pads) in  
19 order to decrease the area of the chip, and

20 when prime factors for  $N$  are 2 and 3 only, the number  $M$  of the  
21 gate-selecting lines is positive and is the smallest integer, next smaller  
22 integer, third smaller integer, fourth smaller integer, or fifth smaller integer  
23 that satisfies the expression  $L/\{(N/M) + M\} > p$ .

1 7. (Twice Amended) A light-emitting thyristor matrix array  
2 formed on a chip, comprising:

3  $N$  ( $N$  is an integer  $\geq 2$ ) three-terminal light-emitting thyristors  
4 arrayed in one line in parallel with the long side of the chip;

5 a common terminal to which cathodes or anodes of the  $N$  light-  
6 emitting thyristors are connected;

7  $M$  ( $M$  is an integer  $\geq 2$ ) anode-selecting lines or cathode-  
8 selecting lines; and

9  $\{(N/M)+M\}$  bonding pads arrayed in one line in parallel with the  
10 long side of the chip,

11 wherein the anode or cathode of  $k$ th light-emitting thyristor is  
12 connected to  $i$ th  $[i=\{(k-1) \text{ MOD } M\} + 1]$  anode-selecting line  $A_i$  or cathode-  
13 selecting line  $K_i$ , where "MOD" in an equation means modulo division,

14 the gate of the  $k$ th light-emitting thyristor is connected to  $j$ th  
15  $[j=\{(k-i)/M\} + 1]$  gate terminal  $G_j$ ,

16 the number  $M$  of the anode-selecting lines or cathode-selecting  
17 lines is selected to satisfy the expression of  $L/\{(N/M)+M\} > p$  ( $L$  is a length of  
18 the long side of the chip and  $p$  is a critical value of array pitch of the bonding  
19 pads) in order to decrease the area of the chip, and

20 when a prime factor for  $N$  is 2 only,  $M$  is positive and is the  
21 smallest integer, next smaller integer, or third smaller integer that satisfies  
22 the expression  $L/\{(N/M)+M\} > p$ .

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1 11. (Twice Amended) A light-emitting thyristor matrix array  
2 formed on a chip, comprising:

3  $N$  ( $N$  is an integer  $\geq 2$ ) three-terminal light-emitting thyristors  
4 arrayed in one line in parallel with the long side of the chip;

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cmt.  
5 a common terminal to which cathodes or anodes of the N light-  
6 emitting thyristors are connected;

7 M (M is an integer  $\geq 2$ ) anode-selecting lines or cathode-  
8 selecting lines; and

9  $\{(N/M)+M\}$  bonding pads arrayed in one line in parallel with the  
10 long side of the chip,

11 wherein the anode or cathode of kth light-emitting thyristor is  
12 connected to ith  $[i=\{(k-1) \text{ MOD } M\}+1]$  anode-selecting line  $A_i$  or cathode-  
13 selecting line  $K_i$ , where "MOD" in an equation means modulo division,

14 the gate of the kth light-emitting thyristor is connected to jth  
15  $[j=\{(k-i)/M\}+1]$  gate terminal  $G_j$ ,

16 the number M of the anode-selecting lines or cathode-selecting  
17 lines is selected to satisfy the expression of  $L/\{(N/M)+M\}>p$  (L is a length of  
18 the long side of the chip and p is a critical value of array pitch of the bonding  
19 pads) in order to decrease the area of the chip, and

20 when prime factors for N are 2 and 3 only, M is positive and is  
21 the smallest integer, next smaller integer, third smaller integer, fourth  
22 smaller integer, or fifth smaller integer that satisfies the expression  
23  $L/\{(N/M)+M\}>p$ .

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1                    12. (Twice Amended) A driver circuit for driving the light-  
2 emitting thyristor matrix array according to any one of claims 1 or 6,  
3 comprising:  
  
4                    a circuit for driving the gate-selecting lines; and  
  
5                    a circuit for driving the anode terminals or cathode terminals;  
  
6                    wherein the circuit for driving the gate-selecting lines including  
7 an even number of gate-selecting signal output terminals and a circuit for  
8 outputting a "selecting" signal to one of the gate-selecting signal output  
9 terminals and "no-selecting" signal to the others of the gate-selecting signal  
10 output terminals, with the terminal to which the "selecting" signal is supplied  
11 being switched in turn.

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